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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/589,595	08/15/2006	Hyun-Ju Park	SUN-0166	2680

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/589,595	PARK, HYUN-JU	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,10-12,22,26,36* is/are rejected.

7)☒ Claim(s) *5,6,8,9,13-21,23-25,27-35 and 37-39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/589,595 filed 08/15/2006 and amendment filed 10/31/2008.

2. Claims 1-39 remain pending in the Application.

3. Applicant's arguments have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 7, 10-12, 22, 26, 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (US Patent 7,185,295).

With respect to claim 1 Park et al. teaches a chip design verification apparatus for verifying a target unit including at least hardware block (within chip testing apparatus shown on the Fig. 2 (col. 5, ll.29-30; abstract), wherein target 34 shown on the Fig. 2 comprises hardware block (col. 5, ll.41-45)), the chip design verification apparatus comprising:

computer including at least one software block in data communication with the at least one hardware block, and which verifies an operation between the at least one hardware block and the at least one software block (within a computer mainframe 2

shown on the Fig. 2, which includes CPU 10 shown on the Fig. 1 (col. 5, ll.1-3), wherein mainframe 2 includes chip testing program 30/software block to communicate with target 34 as shown on the Fig. 2 (col. 5, ll.33-34) for performing a verification of the target (col. 17, ll.19-24),), the computer comprising:

an interface means of transmitting output data of the hardware block, determining whether output data of the software block is valid, and applying only valid output data of the software block to the hardware block (within interface 32 shown on the Fig. 2, which implements a communication data between testing program 30/software and target 34 including hardware, i.e. transmits the test vector to the target 34 and transmits the result back to the testing program 30 (col. 17, ll.49-51) and when the input data is consistent with expected data (i.e. valid data) is kept as shown by step 370 of the Fig. 14a (col. 17, ll.55-56; ll.33-36), wherein expected data (i.e. valid data) is kept by storing in the interface 32 and then applied to the target 34 (col. 12, ll.35-41) using the target interface 74 of the controller 42 of the interface 32 shown on the Fig. 5, which controls an interface 32 for data input and output operations of the target 34 (col. 8, ll.16-18; 20-22));

a storage means of storing the at least one software block and a chip design verification program for verifying the at least one software block (within hard disk 22 shown on the Fig. 1 presenting a computer system for implementation of the verification process of the chip design, wherein hard disk 22 of the mainframe 2 (Fig. 2) stores testing program 30 (Fig. 2) including various of input/output data (col. 5, ll.36-38; ll.10-12)); and

a controller for transmitting the output data of the software block generated by an operation of executing the chip design verification program to the interface means, determining whether the output data of the at least one hardware block input via the interface means is valid, and applying only valid output data of the hardware block to the at least one software block (within controller 42 of the interface 32 shown on the Fig. 5 (col. 6, ll.55-56; ll.3-6), wherein interface 32 implements applying a signal to the target 34 (hardware block) and storing a signal applied from the target 34 /hardware block (col. 8, ll.31-33), wherein chip testing program runs by a normal termination of an operation when the last frame is completely transmitted/valid/kept in step 370 of the Fig. 14a (col. 17, ll.55-56; col. 7, ll.1-3), wherein expected data (i.e. valid data) is kept by storing in the interface 32 and then applied to the target 34 (col. 12, ll.35-41), wherein the target interface 74 of the controller 42 of the interface 32 shown on the Fig. 5, which controls an interface 32 for data input and output operations of the target 34 (col. 8, ll.16-18; 20-22)).

With respect to claim 11 Park et al. teaches the limitations similar to claim 1 including a chip verification method for a chip design verification apparatus including et least one hardware block and a processing means, the processing means having at least one software block, a chip design verification program, and storage means of storing input and output data, and interface means of interfacing with the software block and the hardware block (abstract, title).

With respect to claim 26 Park et al. teaches a data communication method for a chip design verification apparatus for verifying a target unit including a hardware block,

including a software block having at least one function block, a chip design verification program for verifying operations of the software block and the hardware block, a storage means of storing input and output data of the software block generated by executing the chip design verification program, and an interface means of performing an interfacing operation between the hardware block and the software block (abstract, title), the method comprising:

a clock generation step of allowing the chip design verification program to obtain a multi clock setting value to be provided to the interface means, and generate multi clocks in response to a system clock of the chip design verification program and the multi clock setting value to be applied to the software block, and allowing the interface means to generate multi clocks in response to the system clock of the interface means and the multi clock setting value to be applied to the hardware block (within clock controller 66 shown on the Fig. 5, which is a controller of the interface 32 and generates clock signals of the interface 32 (col. 7, ll.59-62), which is in conjunction with controller 64 performs verification/matching step between hardware block/target 34 and software block using interface 32 (col. 18, ll.12-21));

a software side operation step of transmitting output data generated by the operation of the software block operating in response to the multi clocks of the chip design verification program to the interface means, determining whether the output data of the hardware block received via the interface means is valid by executing the chip design verification program, and applying only the valid output data of the hardware block to the software block (by applying multiple clock signals to the target 34 (col. 18,

ll.18-21) and storing data outputted from the target 34 for analysis (col. 18, ll.38-43) and for further determination error identification (col. 18, ll.49-50)); and

a hardware side operation step of transmitting output data generated by the operation of the hardware block operating in response to the multi clocks of the interface means to the software block, determining whether the output data of the software block received is valid by executing the chip design verification program in the interface means, and applying only the valid output data of the software block to the hardware block (by applying multiple clock signals to the target 34 (col. 18, ll.18-21) and storing data outputted from the target 34 for analysis (col. 18, ll.38-43) and for further determination error identification (col. 18, ll.49-50; ll.51-60)).

With respect to claims 2-4, 7, 10, 12, 22, 26, 36 Park et al. teaches

Claim 2: wherein the chip design verification program has a graphic user interface, and allows data transceived by executing the chip design verification program to be displayed via the graphic user interface (col. 4, ll.23-25; col. 7, ll.24-47; Fig. 9);

Claims 3, 12: wherein the chip design verification program obtains a multi clock setting value for operating the software block and the hardware block, and stores the value in the interface means (col. 7, ll.59-62; col. 18, ll.12-21);

Claims 4, 12: wherein the interface means has a clock controller of generating multi clocks in response to the multi clock setting value and a system clock of the interface means and applying the multi clocks to the hardware block (col. 18, ll.12-21);

Claim 7: wherein the chip design verification program generates multi clocks in response to the multi clock setting value and the system clock of the chip design

verification program to apply the multi clock to the software block (col. 7, ll.43-47; col. 18, ll.18-21);

Claims 10, 22, 36: wherein the software block has a test-bench, and the test-bench supplies the multi clock setting value to the chip design verification program and operates in response to the multi clocks of the chip design verification program instead of the multi clocks owned by the test-bench itself (col. 14, ll.27-33);

Allowable Subject Matter

6. Claims 5, 6, 8, 9, 13-21, 23-25, 27-35, 37-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach wherein the output data of the hardware block has an output value of the hardware block changed in response to the multi clocks applied from the interface means, and a system clock count value of the interface means when the output value of the hardware block is changed (claims 5, 13, 27); wherein the valid output data of the hardware block is an output value of the hardware block when the system clock count value of the interface means is equal to or smaller than the system clock count value of the chip design verification program, and is an output value of the hardware block when the output value of the software block is not changed even when the system clock count value of the chip design verification program is increased so as to be equal to the system clock count value of the interface means after determination that the system clock count value of the interface means is greater than the system clock count value of the chip design verification program

(claims 6, 14, 28); wherein output data of the software block has an output value of the software block changed in response to the multi clocks applied from the chip design verification program, and a system clock count value of the chip design verification program when the output value of the software block is changed (claims 8, 15, 29); wherein the valid output data of the software block is an output value of the software block when the system clock count value of the chip design verification program is equal to or smaller than the system clock count value of the interface means, and is an output value of the software block when the output value of the hardware block is not changed even when the system clock count value of the interface means is increased so as to be equal to the system clock value of the chip design verification program after determination that the system clock count value of the chip design verification program is greater than the system clock count value of the interface means (claims 9, 16, 30) among with the limitations of claims from which claims depend.

Remarks

7. In remarks Applicant argues in substance:

a) Thus Park does not teach or suggest "an Interface means of transmitting output data of the hardware block, determining whether output data of the software block is valid, and applying only valid output data of the software block to the hardware block.... and a controller for transmitting the output of the software block to the hardware block... and applying only output data of the at least one hardware block to the at least one software block

b) Park does not teach or suggest "a multi clock setting value for operating the software block and the hardware block" (acclaim 3) or "generating multi clocks in response to the multi clock setting value" (claim 4)

It has to be noted that in Applicant's arguments the name of prior art was erroneously used Clark instead Park (e.g. page 31, 32). Examiner considered it as typographical error.

8. Examiner respectfully disagrees for the following reasons:

With respect to a) Park teaches interface 32 shown on the Fig. 2, which implements a communication data between testing program 30/software and target 34 including hardware, i.e. transmits the test vector to the target 34 and transmits the result back to the testing program 30 (col. 17, ll.49-51) and when the input data is consistent with expected data (i.e. valid data) is kept as shown by step 370 of the Fig. 14a (col. 17, ll.55-56; ll.33-36), wherein expected data (i.e. valid data) is kept by storing in the interface 32 and then applied to the target 34 (col. 12, ll.35-41) using the target interface 74 of the controller 42 of the interface 32 shown on the Fig. 5, which controls an interface 32 for data input and output operations of the target 34 (col. 8, ll.16-18; 20-22).

With respect to b) Park teaches clock controller 66 shown on the Fig. 5, which is a controller of the interface 32 and generates **clock signals**/multi clock of the interface 32 (col. 7, ll.59-62), which is in conjunction with controller 64 performs verification/matching step between hardware block/target 34 and software block using interface 32 (col. 18, ll.12-21), wherein the clock controller 66 receives signals from PCI

bus, the external clock generator, and so on to generate internal and external clock signals of the interface means 32 (col. 7, ll.59-67).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is (571)272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HR
01/30/2009

/Helen Rossoshek/
Primary Examiner, Art Unit 2825